WHAT IS CLAIMED IS:

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1. A method of aligning instructions in a processor comprising:

aligning a first instruction;

decoding the size of the first instruction;

determining the beginning of a second instruction based on the size of the first instruction;

decoding the size of the second instruction;

determining whether processing the second instruction will deplete one of a plurality of buffers; and

instructing the one of the plurality of buffers to receive additional data if processing the second instruction depletes the one of the plurality of buffers.

2. The method of Claim 1, further comprising storing the plurality of instructions in a plurality of sub-buffers.

3. The method of Claim 1, further comprising comparing a most significant bit of a pointer to a first of the plurality of sub-buffers to a most significant bit of a pointer to a second of the plurality of sub-buffers to

determine whether processing one of the plurality of instructions will deplete a buffer.

4. The method of Claim 1, further comprising storing a first instruction across a plurality of storage elements prior to processing the instructions.

5. The method of Claim 1, further comprising adding the size of the first instruction to a current instruction position to determine the beginning of the second instruction.

6. The method of Claim 1, further comprising aligning ahead a number of cycles equal to a cache latency.

7. The method of Claim 1, further comprising aligning instructions in a digital signal processor.

8. The method of Claim 1, further comprising issuing a request to a memory to reload the plurality of buffers.

9. A method of processing instructions within a processor comprising:

predicting whether one of a plurality of buffers will be depleted of instruction data within a number of cycles approximately equal to a cache latency;

preparing the one of a plurality of buffers to be loaded with additional instruction data if the one of the plurality of buffers will be depleted.

10. The method of Claim 9, further comprising decoding the size of the a first instruction in the instruction data;

determining the beginning of a second instruction in the instruction data based on the size and position of the first instruction; and

decoding the size of the second instruction.

11. The method of Claim 9, wherein the plurality of buffers are divided into a plurality of sub-buffers.

12. The method of Claim 11, wherein the predicting is accomplished by comparing a most significant bit of a pointer to a first of the plurality of sub-buffers to a most significant bit of a pointer to a second of the plurality of sub-buffers to determine whether processing one of the plurality of instructions will deplete one of a plurality of buffers.

13. The method of Claim 9, further comprising aligning the instruction data.

14. The method of Claim 9, further comprising processing the instructions in a digital signal processor.

15. The method of Claim 9, further comprising issuing a request to reload the plurality of buffers.

16. A processor comprising:

a plurality of buffers adapted to store first instruction data including a plurality of instructions;

an instruction request unit adapted to align the plurality of instructions for execution;

a width decoder adapted to determine the size of the plurality of instructions;

a transition detector adapted to predict when one of the plurality of buffers will be empty, the transition detector adapted to send a signal to instruct one of the plurality of buffers to load a second instruction data.

17. The processor of Claim 16, wherein the plurality of buffers is divided into a plurality of sub-buffers.

18. The processor of Claim 16, wherein the transition detector compares a most significant bit of a pointer to a first of the plurality of sub-buffers to a most

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significant bit of a pointer of a second of the plurality of sub-buffers to determine whether processing one of the plurality of instructions will deplete a buffer.

19. The processor of Claim 16, wherein the processor aligns ahead a number of cycles equal to a cache latency.

20. The processor of Claim 16, wherein the processor is a digital signal processor.

21. An apparatus, including instructions residing on a machine-readable storage medium, for use in a machine system to align instructions in a processor, the instructions causing the machine to:

receive data containing instructions in a plurality of buffers;

decode the size of a first instruction;

determine the beginning of a second instruction based on the size of the first instruction;

decode the size of the second instruction;

determine whether processing the second instruction will deplete one of the plurality of buffers; and

instruct the one of the plurality of buffers to receive additional data if processing the second instruction depletes the one of the plurality of buffers.

22. The apparatus of Claim 21, wherein the plurality of instructions are stored in a plurality of sub-buffers.

23. The apparatus of Claim 21, wherein a most significant bit of a pointer to a first of the plurality of sub-buffers is compared to a most significant bit of pointer to a second of the plurality of sub-buffers to determine whether processing one of the plurality of instructions will deplete a buffer.

24. The apparatus of Claim 21, wherein a first instruction is stored across a plurality of storage elements prior to processing the instructions.